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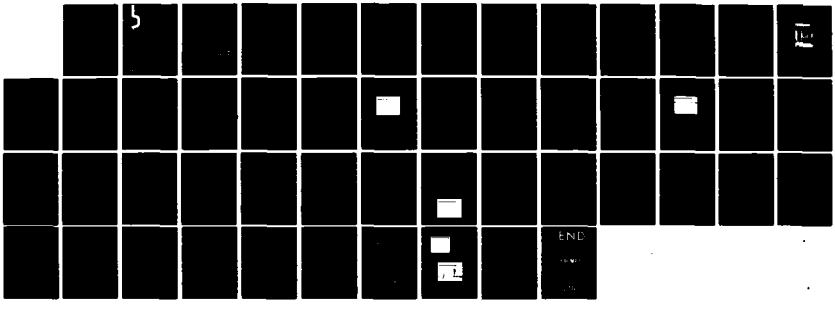

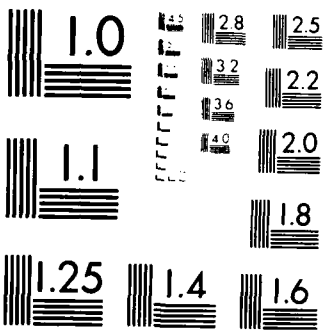

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Annual Technical Report #2

Grant No. AFOSR-82-0344

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Unclassified
SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: UNCLASSIFIED	1b. RESTRICTIVE MARKINGS: N/A
2a. SECURITY CLASSIFICATION AUTHORITY: N/A	3. DISTRIBUTION/AVAILABILITY OF REPORT: N/A
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A	
4. PERFORMING ORGANIZATION REPORT NUMBER(S): N/A	5. MONITORING ORGANIZATION REPORT NUMBER(S): N/A
6a. NAME OF PERFORMING ORGANIZATION: UNIVERSITY OF CALIFORNIA Santa Barbara Campus; 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION: AFOSR Bolling AFB, Dr. Gerald Witt
6c. ADDRESS (City, State and ZIP Code): Electrical & Computer Engineering, University of California, Santa Barbara, CA 93106	7b. ADDRESS (City, State and ZIP Code): AFOSR/NE, Building 410, Bolling Air Force Base, DC 20332
8a. NAME OF FUNDING/SPONSORING ORGANIZATION; 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State and ZIP Code)	10. SOURCE OF FUNDING NOS. — PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT NO.
11. TITLE (Include Security Classification): DEVELOPMENT OF A PLANAR HETEROJUNCTION BIPOLAR TRANSISTOR FOR VERY HIGH SPEED LOGIC	
12. PERSONAL AUTHOR(S): Stephen I. Long	
13a. TYPE OF REPORT: Annual; 13b. TIME COVERED: FROM 10/1/83 TO 9/30/84	14. DATE OF REPORT (Yr., Mo., Day): November 21, 1984; 15. PAGE COUNT: 47
16 SUPPLEMENTARY NOTATION	
17. COSATI CODES — FIELD / GROUP / SUB. GR.	18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

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20 DISTRIBUTION/AVAILABILITY OF ABSTRACT: UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS ☐	21. ABSTRACT SECURITY CLASSIFICATION: UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL: STEPHEN I. LONG	22b TELEPHONE NUMBER (Include Area Code): (805) 961-3965; 22c OFFICE SYMBOL

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

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Annual Technical Report #2. Grant No. AFOSR-82-0344

Development of a Planar Heterojunction Bipolar Transistor for Very High Speed Logic

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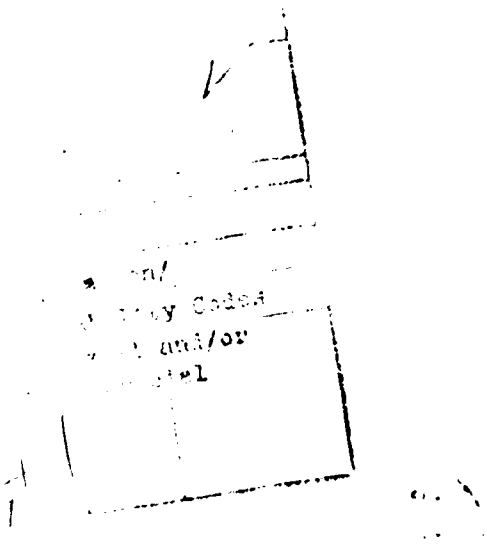
ABSTRACT

The objective of this research project is to develop heterostructure bipolar transistors for very-high-speed logic. During the second year of effort, significant progress was made on (Aℓ,Ga)As/GaAs HBTs of both emitter-down and emitter-up configurations, with current gains of 10 or greater being observed in both cases for base dopings which exceed emitter dopings. Structural modifications were evaluated which led to increased injection and reduced recombination currents. Annealing systems were constructed and characterized for activation of Be ion-implantations. Promising initial studies of (In,Ga)P/GaAs HBTs has led to their inclusion in this research project for the third year of effort.



1. RESEARCH WORK STATEMENT

The objective of this research project is to develop heterojunction bipolar transistors in the (Aℓ,Ga)A/GaAs and (In,Ga)P/GaAs material systems for very-high-speed logic applications. The original statement of work from the proposal is repeated below to describe in more detail the nature of the anticipated specific tasks. Progress on the project during the second year is reported in Section 2; related work partially supported by this project will be reported in Appendices A and B.

1.1 MBE Growth on Non-Integrated HBT Structures

This first objective consists of a learning phase, where the more familiar (Aℓ,Ga)As/GaAs material system is used to fabricate discrete single heterojunction bipolar transistor structures. Conventional mesa-etch techniques will be used for isolation and exposure of the base region for contacting. Characteristics of the wide-gap emitter junction will be determined, and transistor action will be evaluated. These initial studies will help to provide insight into HBT fabrication requirements and will provide an initial baseline against which the results of subsequently fabricated more complex devices and material systems can be gauged.

1.2 MBE Growth of InGaP on GaAs

The second objective will be to investigate MBE growth of InGaP on GaAs and GaAs on InGaP. This will include:

a) Pre-MBE Substrate Preparation. The effects of various surface treatments such as chem-mechanical polishing, chemical etching, and in-situ anneal-

ing on subsequent epitaxial deposition will be systematically studied. It is expected that procedures similar to those already developed for GaAs/GaAs or GaAs/(Aℓ,Ga)As growth will be applicable.

b) MBE Growth Parameters. The influence of substrate temperature and P_2 flux on the epitaxial InGaP layer quality will be determined. This includes specifically a determination of the interrelation between Ga and In source temperatures to yield the correct Ga:In flux ratio for lattice matching. At a later stage, coaxial sources will be developed, possibly also mixed sources. In-situ RED patterns can be of value in monitoring initial nucleation and post-nucleation structural changes. Photoluminescence measurements can be used to determine composition and evaluate interface strain (related to peak width) Auger analysis and sputter-Auger profiling can also be employed to determine composition of the film.

c) Electrical Properties. Conductivity and Hall effect measurements at temperatures from above room temperature down to at least liquid nitrogen temperature will be performed to evaluate the quality of deposits. Both isotype and anisotype heterointerfaces will be evaluated by: (1) I-V measurements vs. temperature; (2) C-V measurements, either through self-capacitance of the heterojunction or by profiling through the interface from an adjacent p-n junction or Schottky barrier.

1.3 Horizontal Definition of Transistor Structures

The third objective will be to fabricate heterojunction and double-heterojunction bipolar transistor structures on semi-insulating GaAs substrates while evaluating a variety of techniques for horizontal isolation and patterning of transistor islands. Some parts of this task can be carried out in parallel with the MBE growth task. This task includes:

a) Ion Implantation into InGaP and GaAs. Both p-type doping of InGaP and isolation by bombardment with protons or B^+ or O^+ will be evaluated. Beryllium as a p-type doping species is expected to be effective in achieving high levels of net acceptors in (In,Ga)P. Investigation of the electrical isolation achievable by ion implantation will involve study and electrical characterization through appropriate test structures. The effect of: (1) damage species; (2) implant conditions (energy, dose, temperature); (3) post-implant annealing will be explored. Annealing caps such as Si_3N_4 will be evaluated for activation efficiency of the Be-dopant. Conductivity and hole mobility will be measured.

b) Low Resistivity Contacts for Base and Emitter. While familiar metal systems such as Au-Ge/Ni/Au and Au-Zn are known to provide adequate contact resistance on n+ and p+ GaAs respectively, the advantages of a self-aligned structure which could come from a single contact metallization are great. Therefore, alternatives such as grading and lower bandgap surface layers may be explored as time permits.

c) Selective Epitaxy. The applicability of epitaxial growth in localized surface areas for isolation amd patterning of transistor structures will be determined. Growth of InGaP on GaAs or GaAs on InGaP will be attempted in selected surface regions using Si_3N_4 or polycrystalline Ge as a growth-masking material. Patterning of the work materials will be accomplished by plasma etching. The morphology and electrical characteristics of these locally-grown layers and their interfaces will be evaluated and optimized experimentally. Methods for surface protection (such as polycrystalline As) will be developed if needed.

d) Fabrication of HBT Test Structures. Heterojunction bipolar transistors will be defined in the MBE-grown epitaxial films by conventional methods

(photolithography, mesa etching) for the purpose of providing transistor-like structures for testing. These devices will be used to evaluate (1) injection vs. interface recombination currents (HJ emitters); or (2) band edge discontinuities and interface charges (collectors).

1.4 Device Characterization and Optimization

Demonstration devices that are fabricated by the first three tasks will be fully characterized for all dc parameters. The injection efficiency, the common-base current gain α, and common emitter current gain β, will be measured as a function of temperature, bias conditions, and doping levels in the emitter and base. Critical evaluation of the comparative advantages and disadvantages of both (Aℓ,Ga)As/GaAs and (In,Ga)P/GaAs material systems and their device performance will be carried out. Other material systems might also be evaluated, but only if the (In,Ga)P performance would suggest the need for further exploration. Both single and double HBTs will be fabricated and characterized if possible.

2. Status of Research

The following sections of this report describe the work which was performed during the second year of this project. Some of the most significant areas of accomplishment during the past year include: (1) Design and evaluation of a new heterojunction bipolar mask set which includes smaller transistors and a variety of materials test structures; (2) (Aℓ,Ga)As/GaAs emitter-up HBTs were fabricated with current gains of 600 at low base dopings and 25 at high base doping; (3) (Aℓ,Ga)As/GaAs inverted (emitter-down) HBTs were fabricated with ion-implantation being used for lateral confinement. A DC current gain of 10 was observed on these devices; (4) The (In,Ga)P/GaAs HBT studies which were initiated under other funding sources* have progressed to the point that work on this promising device and material system should be transferred to the AFOSR project; (5) Construction of both furnace proximity annealing and rapid thermal annealing systems has been completed. Both approaches are being evaluated for Si and Be implantation into III-V compound semiconductors.

2.1 HBT Mask Set (M.A. Rao)

The purpose of the mask set is to support device fabrication and to provide test structures for material and process evaluation.

2.1.1 Device Fabrication

a) Mask Layers. The mask set allows for fabrication of conventional mesa-etched devices and also of planar and inverted HBTs. The mask set has

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* Jointly funded by a "MICRO" grant from University of California, Hewlett-Packard Corp., Rockwell International and Xerox Corp. Prof. H. Kroemer is the principal investigator.

patterns (layers) for 9 processing steps, which are described in detail in sec. 2.2. Briefly, they are the following:

Layer 1. Allows absolute reference features to be etched into the wafer, which serve as alignment marks for subsequent steps. Use of this layer is optional.

Layer 2. The emitter mesa is defined in this layer, along with alignment marks for subsequent steps.

Layers 3 and 4. These layers are used for etching the base and collector mesa, respectively.

Layers 5 and 6. Layer 5 is used to lay down contacts to the emitter and collector, and layer 6 is used to contact the base.

Layer 7. Contact cuts are etched through a dielectric layer (sputtered silicon dioxide or AZ1350J photoresist) using this layer.

Layer 8. Defines the final metallization. All test patterns can be accessed by probe using a standard NBS probe card format (2 × 10).

b) Device Sizes. The emitter sizes of the HBTs are 20μm × 20μm, 20μm × 150μm, and 150μm × 150μm, giving a perimeter to area ratio over an 8 to 1 range. This variation in perimeter to area ratio can be used to investigate current crowding effects and surface recombination effects in the HBTs. Fig. 2.1.1 shows the schematic diagram of a typical device. A scanning electron micrograph of a fabricated device, before the final metallization, is shown in Fig. 2.1.2.

2.1.2 Test Structures of Material and Process Evaluation

The HBT masks allow a number of test structures to be generated during device fabrication. These test structures are used to characterize the electrical properties of the layers and to evaluate the fabrication process. The various test structures and their functions are described in the following.

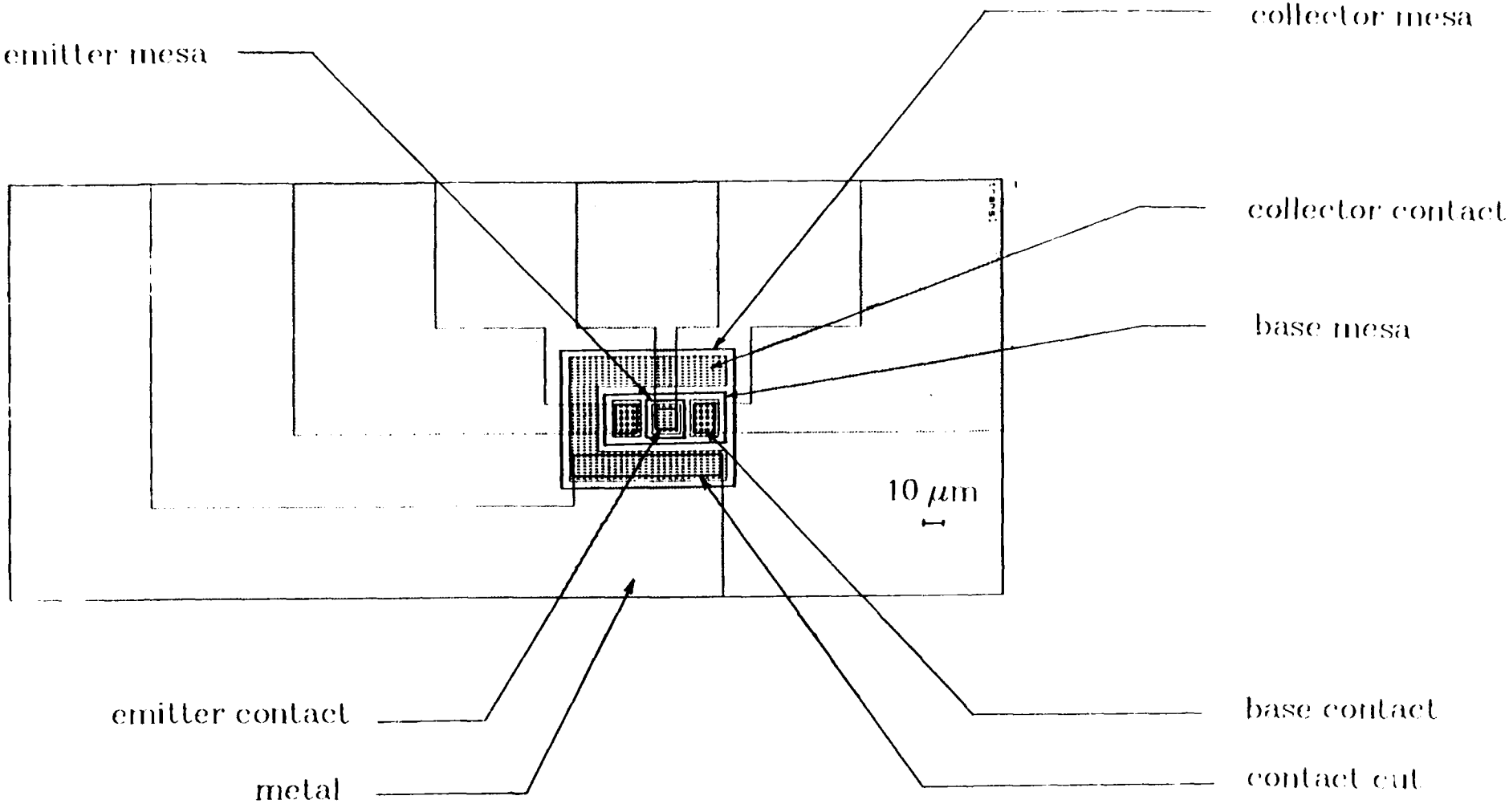

Fig. 2.1.1 HBT: Geometry & probing configuration.
Emitter size: 20 μ x 20 μ.

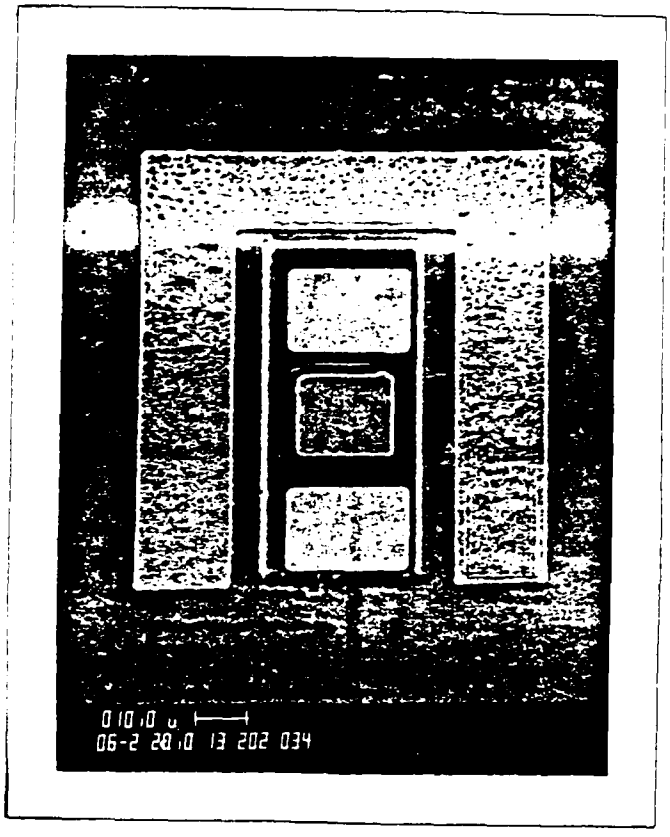

Fig. 2.1.2 SEM micrograph of HBT shown schematically in Fig. 2.1.1. before final metallization.

a) Greek Cross. "Greek crosses" on the emitter, base and collector layers give information on the sheet resistance of each layer. These cross sheet resistors give the same (within 0.5%) measured sheet resistance as conventional van der Pauw structures [1]. This test structure is important in that it allows the accurate measurement of the sheet resistance of a very small region whose width is limited only by the fabrication technology [2]. A schematic diagram of a Greek cross is shown in Fig. 2.1.3. The mask set also has Greek crosses which have been configured for bonding, to enable measurement of resistivity and mobility as a function of temperature.

b) Contact Resistance. Emitter, base and collector contact resistances are measured by a 4-point method described in [3], [4]. A typical test structure is shown in Fig. 2.1.4.

c) C-V Measurements. The mask set provides for three base-collector diodes of different areas, the largest of which (3e-4 cm2) is used for C-V profiling the base-collector junction.

d) High-Frequency Tests. The smallest transistor (emitter size 20μm × 20μm) has been configured for bonding onto a stripline for carrying out high frequency tests.

It was found that the mask set worked satisfactorily. However, it can be seen that the feature sizes are quite large, the smallest device has a collector mesa area of 100μm × 70μm. Also the alignment tolerance is such that the masks can be aligned to within +/ 2μm. With increasing experience in the use of the new Karl Suss MJB3 mask aligner, and with improved photolithographic techniques, we feel that devices with emitter sizes of 4μm × 4μm, with alignment tolerances of +/-0.5μm can be achieved.

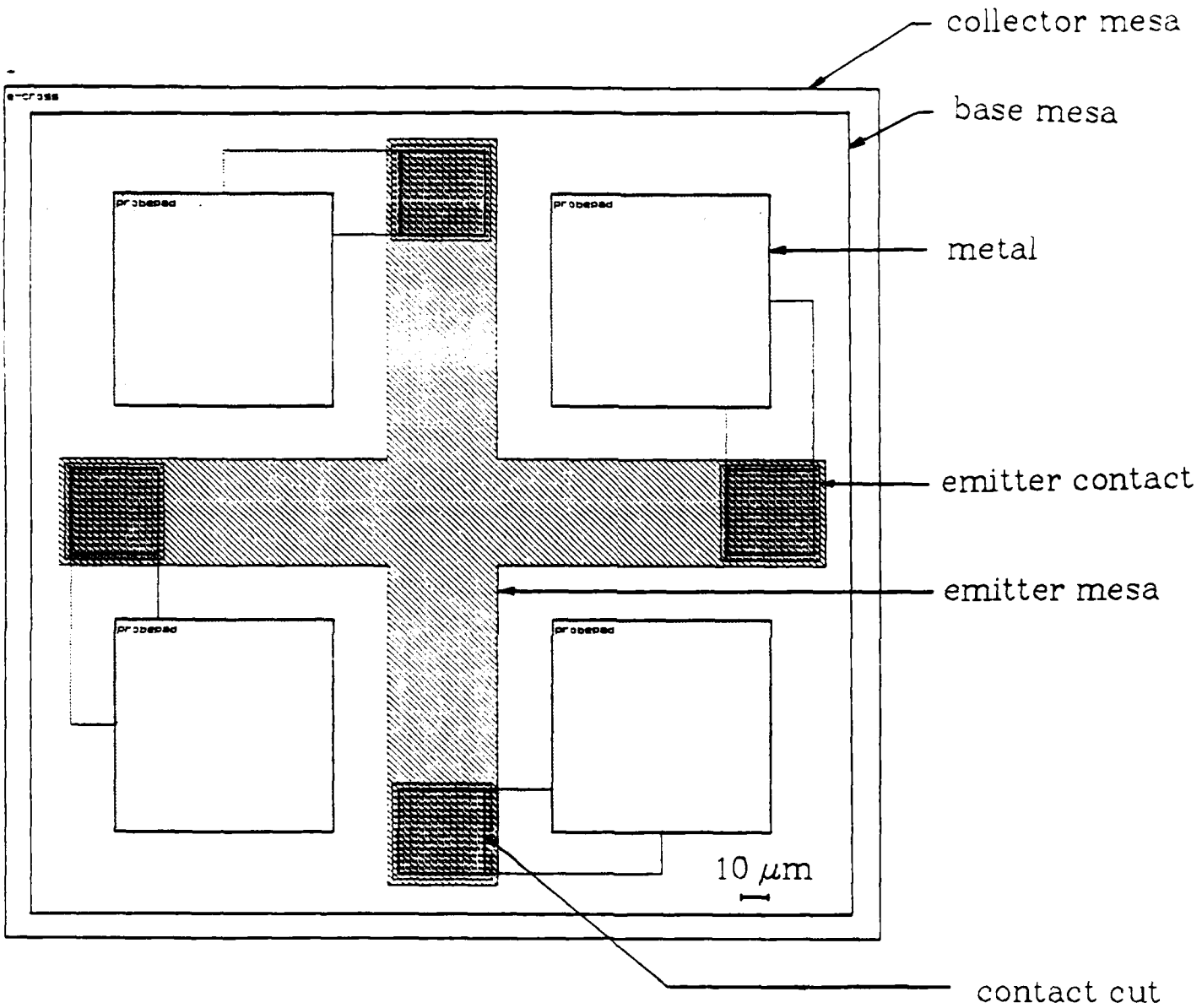

Fig. 2.1.3 Greek cross test structure on the emitter mesa.

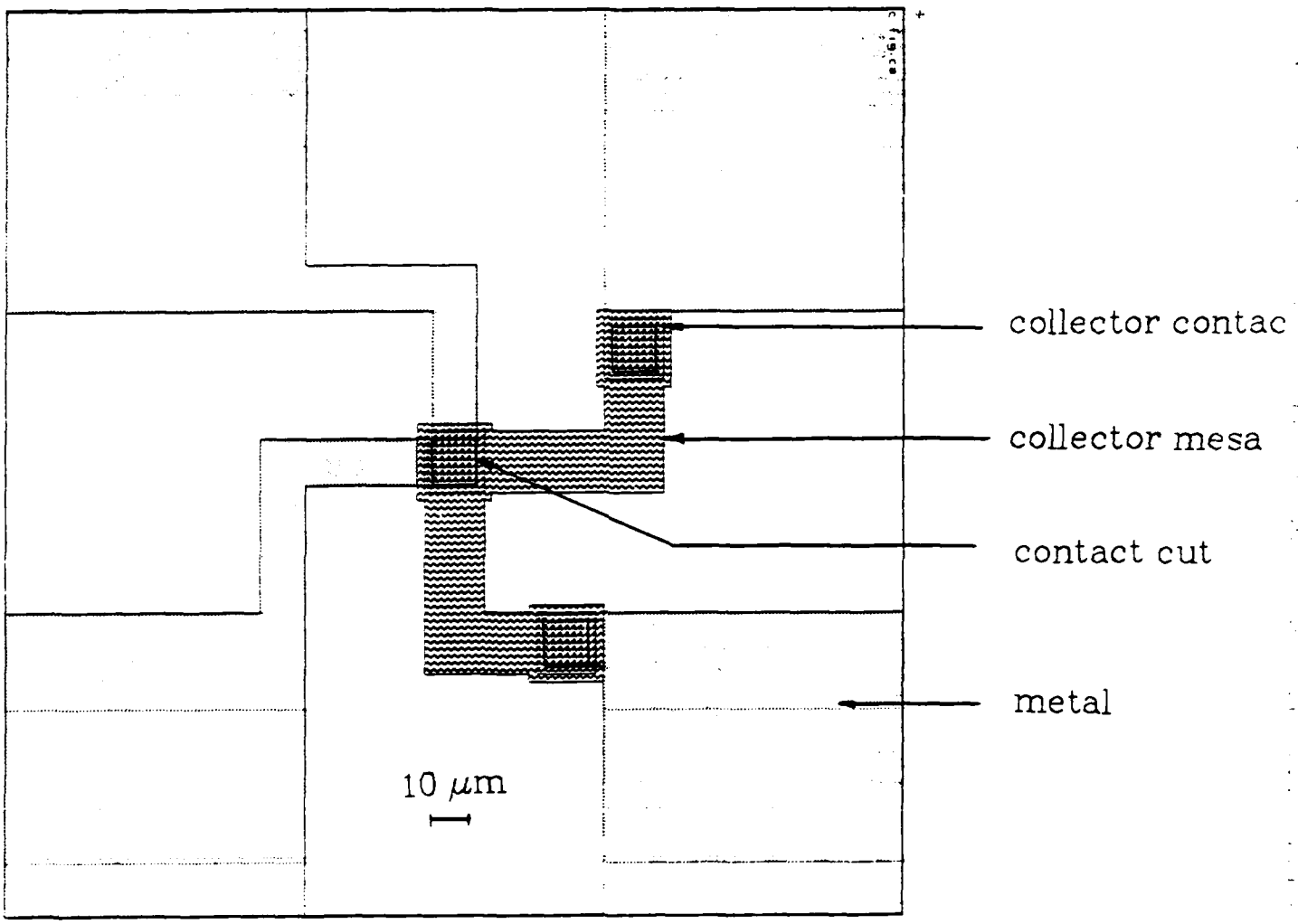

Fig. 2.1.4 Test structure for contact resistance measurement.

2.2 AℓGaAs/GaAs Heterojunction Bipolar Transistor (B. Hancock)

During the past year we have continued work on AℓGaAs bipolar transistors, both in the inverted and the conventional configurations. To review, the band diagram (for either structure) is shown in Fig. 2.2.1, and the basic structures are shown in Fig. 2.2.2. The principle of the wide-gap emitter is that the barrier for injection of holes into the emitter is larger than the barrier for the injection of electrons into the base. Because of this it is no longer necessary to dope the base more lightly than the emitter in order to prevent back injection. This allows the base resistance to be reduced. A graded layer at the emitter-base junction eliminates the spike that would otherwise form in the conduction band, raising the injection barrier for electrons. As long as the grading is entirely within the depletion region, the effective band gap of the emitter is not reduced.

The inverted structure has several advantages. First, it is more suitable for the construction of common emitter circuitry. Second, and more important, the collctor-base area, and hence the collector capacitance, is reduced. In turn, of course, the emitter capacitance is increased. Since the collector is the high impedance side of the circuit, and the emitter the low impedance side, this exchange is a benefit. However, in order to obtain a large current gain it is necessary to restrict the injection to those areas of the base from which it may be collected. To achieve this the wide-gap material under the base contacts is converted to p-type, forming a wide-gap junction with a higher turn-on voltage (i.e. higher barrier to injection).

Although our early device attempts were plagued with processing difficulties, we successfully fabricated an abrupt heterojunction emitter-up transistor with a beta of 600. Common emitter curves are shown in Fig. 2.2.3. Unfortunately, because the base doping of this device was rather low and the

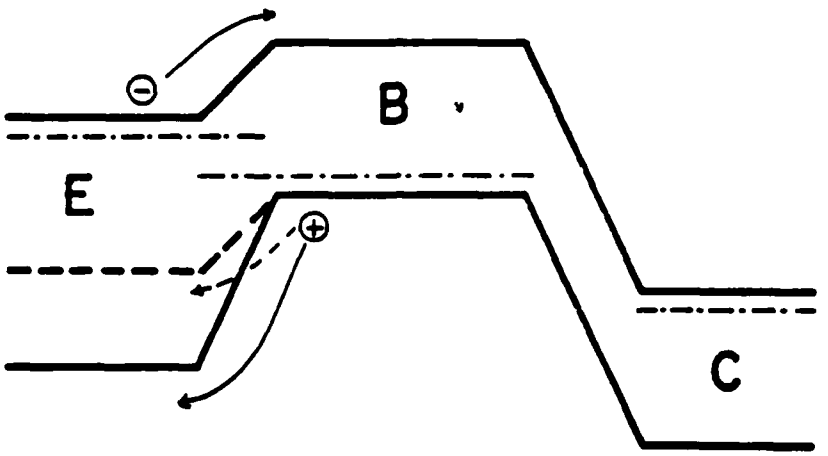

Fig. 2.2.1 Band diagram comparison of homojunction (dashed lines) and heterojunction transistors.

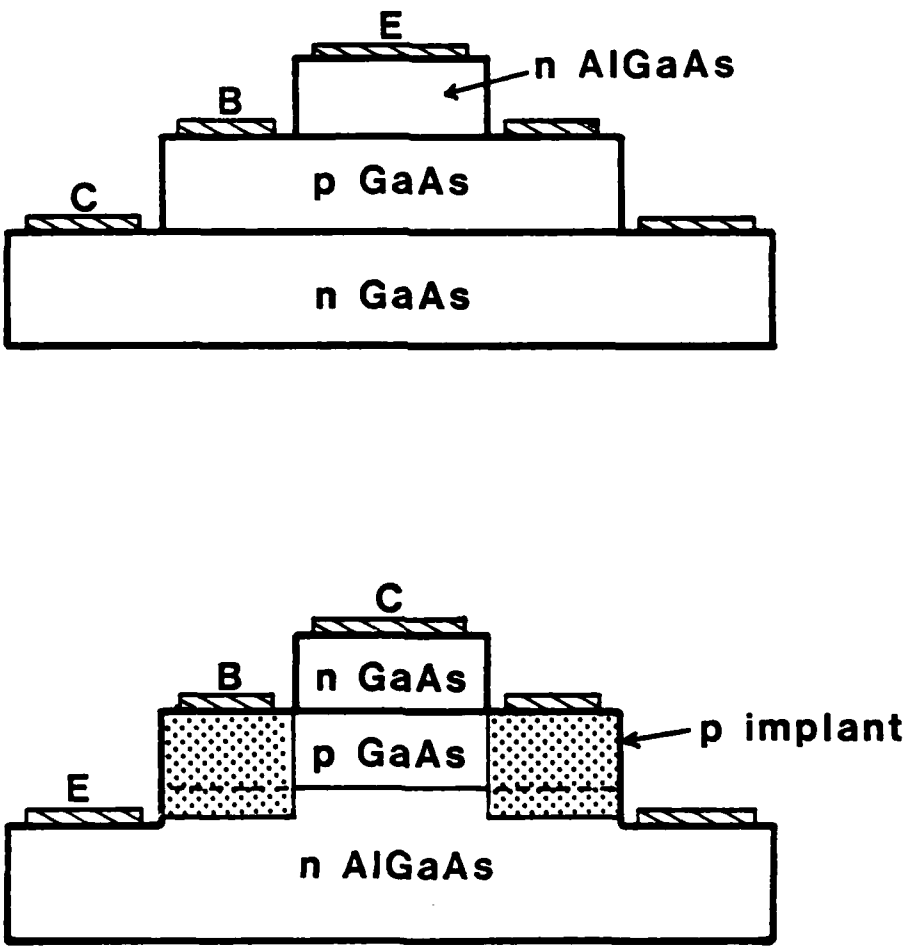

Fig. 2.2.2 a) Basic structure for conventional HBT. b) Basic structure for inverted HBT.

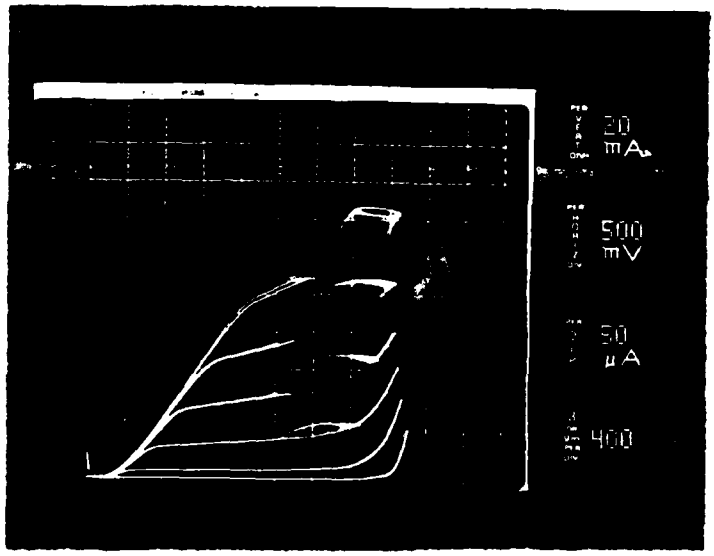

Fig. 2.2.3 Common emitter curves for abrupt heterojunction, emitter-up transistor.

geometries extremely large, this device suffered from severe base resistance, making it unsuitable for further measurement. The new mask and mask aligner made it possible to fabricate much smaller devices. Smaller devices with higher base dopings were fabricated which had current gain of 25 or more. On these devices the base was doped heavily compared to the emitter, demonstrating the wide-gap emitter effect. These devices fell victim to a processing failure so no detailed testing could be done.

The first attempts at making inverted structure transistors suggested that simple abrupt emitter structures were not effective. This may be caused by the deterioration in quality of AlGaAs with increasing layer thickness. It was found that simple p-N junctions, grown on n-type substrates with the p-type layer on top, were very useful as test structures. These can be processed much more quickly and reliably than transistors, allowing a variety of emitter structures to be tested. By plotting log I vs. V one can rapidly discern from the slope (ideality factor) whether the current is carried by injection or recombination. By varying the geometry one can determine whether recombination current is the result of a poor interface or whether it is a surface effect. Finally, by measuring the temperature dependence of such curves, the height of the injecting barrier can be determined. This sensitivity and depth of information is not provided by linear I-V curves (as measured by a curve tracer). Although these measurements can (and should) be made on transistors, current crowding will add a masking effect.

Our first observation was that devices larger than $10^3 cm^2$ were highly inconsistent, suggesting some sort of defect. This was a strong driving factor toward obtaining a mask with finer features.

Fig. 2.2.4 shows log J-V curves for a variety of structures listed in Table I. Layer 97 was a simple abrupt junction. The ideality factor of 2 and

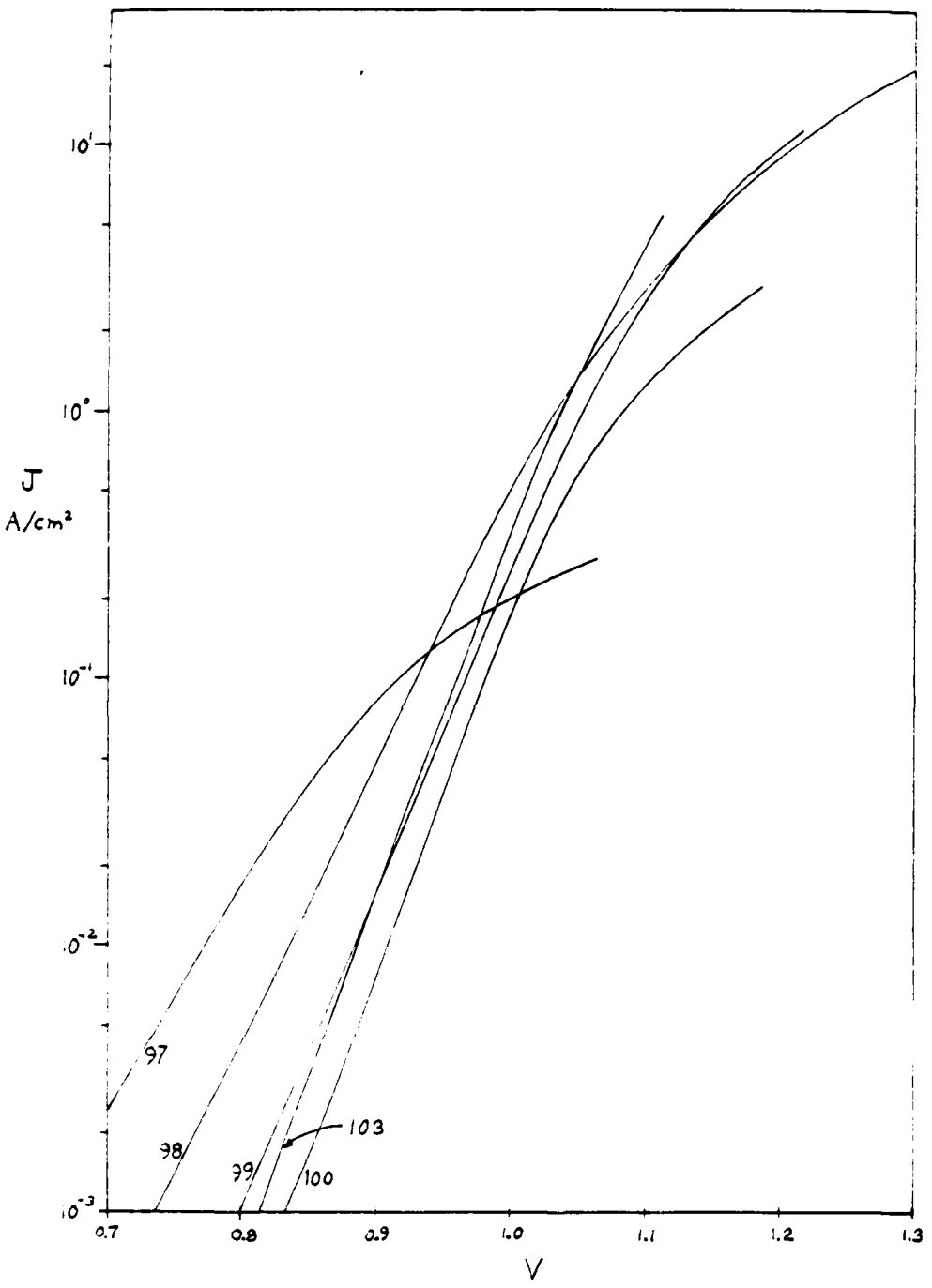

Fig. 2.2.4 Log J-V curves for diodes listed in Table I.

the high current indicate a large amount of recombination. In layer 98, an undoped GaAs layer was introduced to move the location of the recombination peak (where n=p) into the higher quality GaAs. The ideality factor and total current (sum of injection and recombination) is reduced, indicating improvement. In layer 99 the heterojunction was graded linearly. The improvement is drastic. In layer 100 the interface was graded by growing a superlattice with a variable duty cycle. Finally, in layer 103, thin layers of GaAs are introduced periodically into the AℓGaAs. This improves the AℓGaAs, presumably by trapping impurities. Diodes were fabricated with areas from 2×10^{-5} cm^2 to $1\times10^{-3}cm^2$. For all layers the current scaled with the area, indicating minimal surface recombination.

This technique is also useful for evaluating the effectiveness of an implant. Fig. 2.2.5 shows J-V curves for two diodes on the same wafer, one of which was implanted with 100 KeV beryllium to a dose of $5\times10^{14}cm^{-2}$ and annealed at 700°C for 15 minutes. During the anneal an arsenic overpressure was supplied by an InAs source upstream. The injection current in the implanted device should be reduced by six orders of magnitude. The remaining current seen is the recombination (leakage), with an ideality factor of 2. This leakage is especially pronounced at low currents and is probably the result of unannealed defects.

Inverted mode transistors have been fabricated which show a current gain of 10. I-V curves are shown in Fig. 2.2.6. These devices were made with the structure shown in Table II using the implant and anneal described above. It is suspected that the beta is limited by the leakage of the implanted region. Experiments are now under way to optimize the annealing to minimize this leakage.

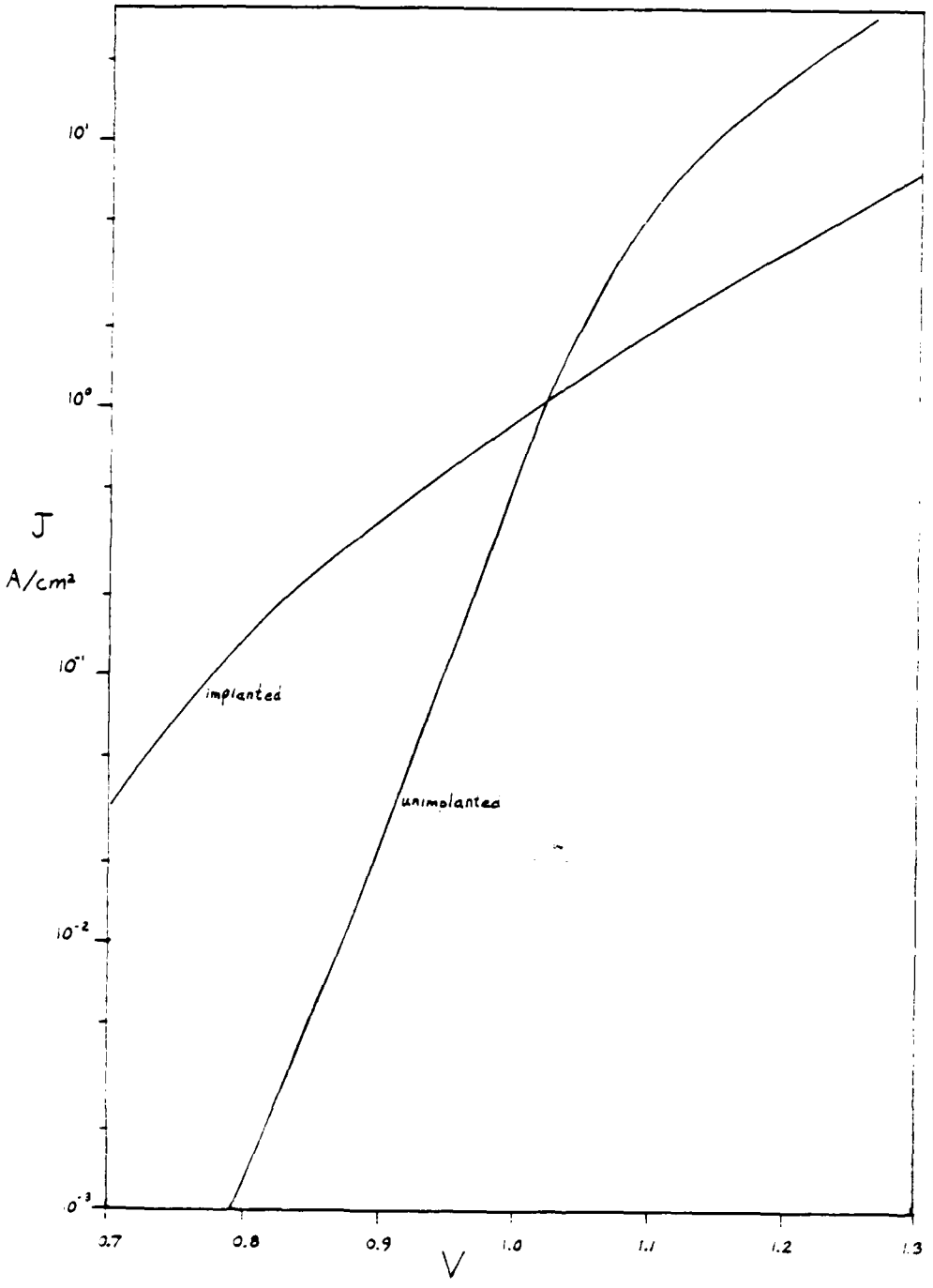

Fig. 2.2.5 Log J-V curves for implanted and unimplanted diodes of layer number 99.

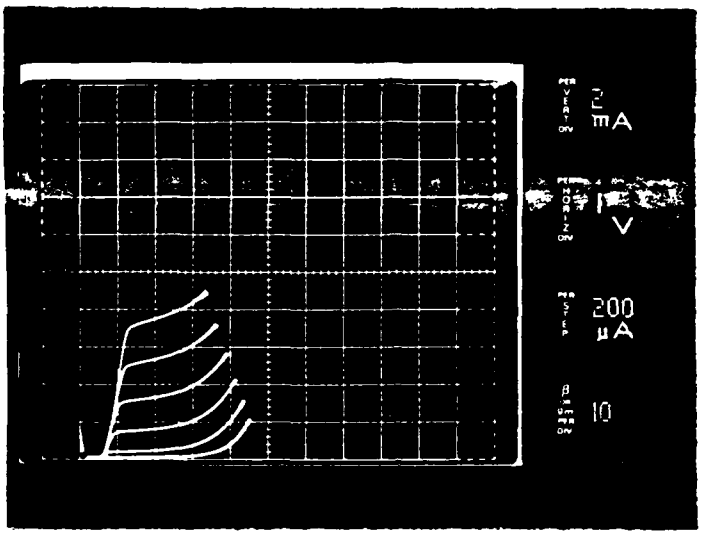

Fig. 2.2.6 Common emitter curves for inverted transistor made with emitter structure layer of number 99.

As indicated before, fabrication of these devices at first proved troublesome. The process is now fairly well established and will be briefly described. Layers are grown by MBE, usually with a substrate temperature of 650°C, growth rate of 0.5μm/hr and atomic flux ratio of about 3. After removal from the MBE system, the indium used for mounting is etched off with warm HCl and the backside lapped flat. The collector mesa is then patterned with positive resist and etched with $1H_2O_2:4H_2SO_4:35H_2O$ through to the base layer. The same photoresist is then used as a mask for the beryllium implant. After removal of the photoresist, the implant is annealed. Next, the base mesa is etched. Au:Sn, Au:Zn, and Au:Ge/Ni for substrate, base and emitter contacts respectively, are evaporated using the liftoff technique and annealed. A dielectric layer of AZ1350 is deposited, patterned, and hard baked at 180°C for 30 minutes. Finally an interconnect layer of Cr/Au is deposited.

For the future, it should be possible to greatly improve the implant and anneal, giving higher current gains. Also, by etching only through the heavily doped collector layer and using a low energy implant to contact the base layer, the etching requirements can be eased and the planarity improved.

Table I

97	2500Å	GaAs	$p=2\times10^{18}$
	1000Å	AℓGaAs	$n=5\times10^{17}$
98	2500Å	GaAs	$p=2\times10^{18}$
	500Å	GaAs	nid
	1000Å	AℓGaAs	$n=5\times10^{17}$
99	2500Å	GaAs	$p=2\times10^{18}$
	500Å	GaAs	nid
	500Å	Graded	nid
	1000Å	AℓGaAs	$n=5\times10^{17}$
100	2500Å	GaAs	$p=2\times10^{18}$
	500Å	GaAs	nid
	150Å	Digital Grade	nid
	1000Å	AℓGaAs	$n=5\times10^{17}$
103	2500Å	GaAs	$p=2\times10^{18}$
	500Å	GaAs	nid
	1000Å	(150Å AℓGaAs, 15Å GaAs)	$n=5\times10^{17}$

Table II

Transistor layer 105 structure

500Å	GaAs	$n=5\times10^{17}$
2500Å	GaAs	nid
2500Å	GaAs	$p=2\times10^{18}$
500Å	GaAs	nid
500Å	Graded	nid
1000Å	AℓGaAs	$n=5\times10^{17}$

2.3 GaInP/GaAs HBT Future Plans (M.A. Rao)

The first Npn HBT using the GaInP/GaAs heterojunction has already been reported [Appendix B]. Common emitter gains of 30 have been attained, with the base doping exceeding the wide gap emitter doping. Atomic Phosphorous to total group III elemental ratios of 30:1 were required for growing the GaInP emitter. Since then, GaInP lattice matched to GaAs to within 0.1%, has been grown at 778 K, with an atomic V to III ratio of 20:1.

Growth of GaP on Si wafers with a 211 orientation shows that surfaces with good morphology can be obtained with low V:III flux ratios [5]. Hence we feel that growth of GaInP on 211-GaAs may require lower Phosphorus fluxes, and we propose to investigate the growth of GaInP on 211-GaAs. Also, we intend to grow GaInP on GaAs at substrate temperatures of 833 K to 853 K, in order to obtain higher quality interfaces than those grown at 778 K.

Mesa etched devices will be fabricated using the new mask sets, and the layers and the process will be characterized. We will also attempt to fabricate planar devices. High frequency tests of the HBT will also be performed. We will also investigate the GaInP/GaAs heterojunction interface by C-V profiling using the newly acquired Polaron semiconductor profiler PN4200, in order to determine the conduction band discontinuity [6], [7].

3. Publications

No publications or presentations were prepared or delivered during the second year of the project. (See Appendix B for related publication)

4. Personnel

Prof. Stephen I. Long is the principal investigator and Prof. H. Kroemer the co-principal investigator. Two graduate research assistants are currently

being supported by this grant. Mr. Bruce Hancock is working on the (Aℓ,Ga)As/GaAs MBE growth, fabrication and characterization of HBT devices. Mr. M.A. Rao was responsible for the design of the new masks and assisted with (Aℓ,Ga)As/GaAs HBT processing. He is currently working on (In,Ga)P/GaAs MBE growth and HBT fabrication. ECE Department staff, Mr. D. Zak, provided support in the solid-state laboratory for development of equipment and facilities.

During the past year, Mr. J. Blokker, also a research assistant on this program, received his MS degree and left UCSB.

Appendix A

Annealing of ion-implanted GaAs (A. Yuen)

It was determined early in the AFOSR program that ion implantation would play an important role in the fabrication of inverted HBT structures. In order to utilize implantation in III-V materials, an annealing system is needed which can control the wafer surface so that neither Ga nor As is lost during the anneal. This AFOSR contract provided equipment funding so that a furnace could be dedicated to furnace annealing with either capped samples or capless with As overpressure. Funding was also provided to purchase a lamp housing and control module for development of a rapid thermal annealing capability. This technique, while less well understood, is potentially more desirable for application to HBT fabrication, because diffusion of p-type base dopants into the emitter would be minimized by the very short time interval at high temperatures. During the past year, both of these objectives have been accomplished. Support for a research assistant to study annealing in III-Vs has been provided by the Semiconductor Research Corporation.* The present status of this work is described below.

The annealing project was initiated at the beginning of this year. Initial stages included the design and construction of a furnace anneal system. This system was very similar in design to one described by Woodall et al. [8] in which an As overpressure is provided in a reduced volume region by thermal decomposition of InAs. InAs has approximately 100 times the As vapor

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* "Core Program on GaAs Digital Device Research," contract No. SRC-84-01-044, Semiconductor Research Corp., Research Triangle Park, NC.

pressure at typical annealing temperatures than GaAs. In order to do some novel comparisons between furnace annealing (FA) and rapid thermal annealing (RTA), the construction of an RTA system was initiated in the spring and was completed during the summer session. A drawing of both of the annealing systems is provided in Fig. A.1.

The types of implantations that have been studied include both n-type (Si) and p-type (Be) implants into semi-insulating GaAs substrates. N-type dopants were implanted with a dose of 5E12 cm2 at an accelerating energy of 100 KeV and p-type dopants were implanted with a dose of 1E14 cm-2 at the same accelerating energy. Various characterizing methods were used to compare the performances of the two annealing methods.

a) Hall Measurements. Determines the activation percentage as well as the Hall mobility. The Hall mobility is a good indication of how effective the anneal was at recrystallizing the damaged lattice.

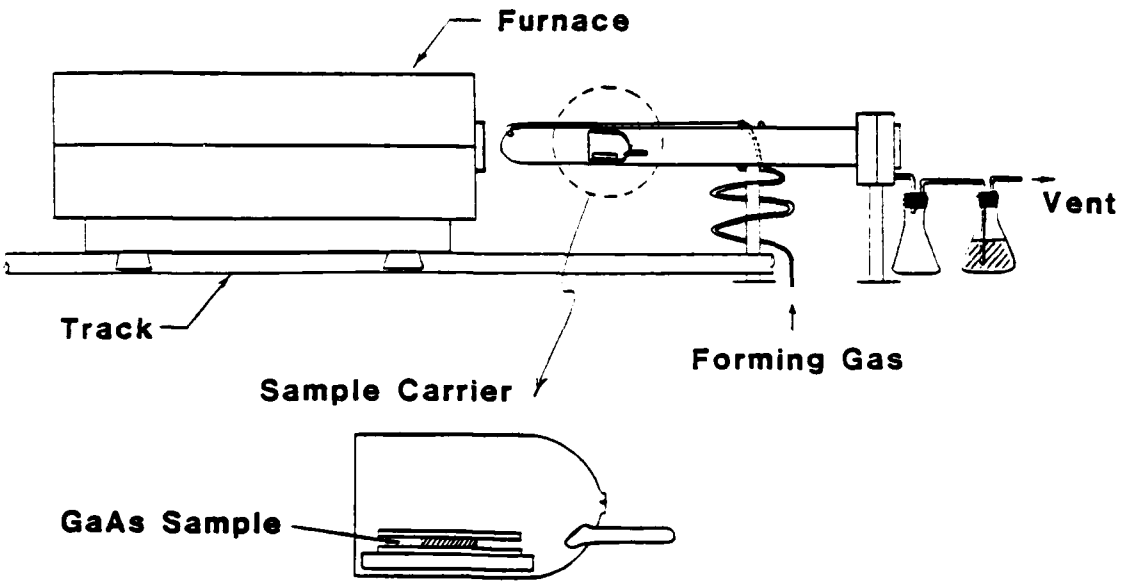
b) CV Measurements. Provides a good approximation of the actual doping profile. The measured profiles can subsequently be compared to LSS theoretical profiles and evaluated accordingly.

c) Photoluminescence (PL). PL data taken before and after annealing provides information on the uniformity of the crystal and the amount of defects still present in the material.

d) Device Measurements. Discrete MESFETs fabricated on implanted samples allows for comparisons to be made between device performance the type of annealing method used.

Results from Hall measurements show that activation percentage of n-type (Si) dopant after RTA to be approximately 20% lower than after FA. On the other hand, the Hall mobility is not significantly different between RTA and FA samples. A possible explanation for this is that Si acts more like an

FURNACE ANNEAL SYSTEM



RAPID THERMAL ANNEAL SYSTEM

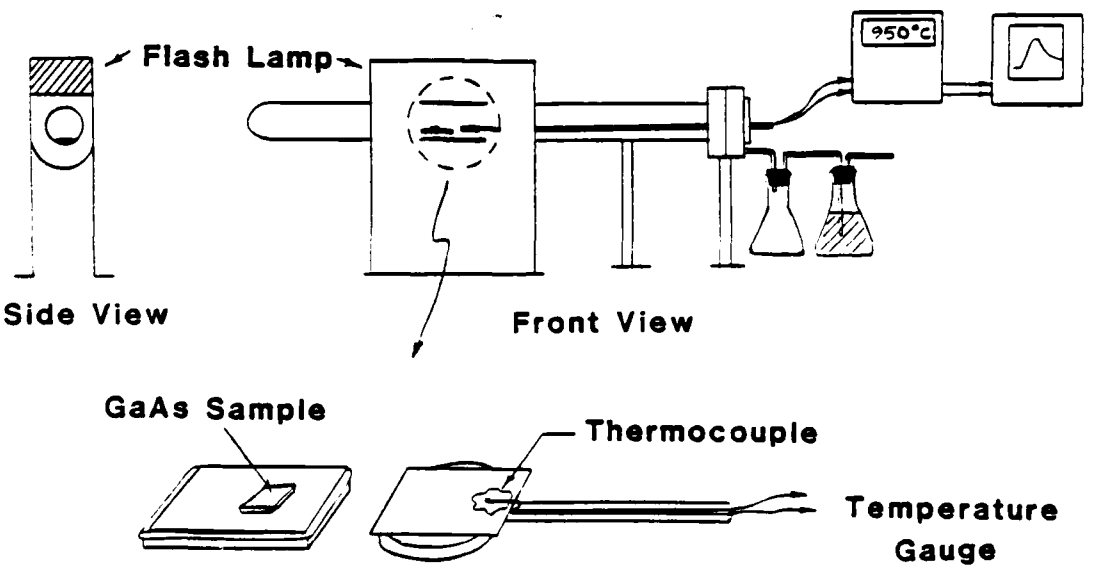
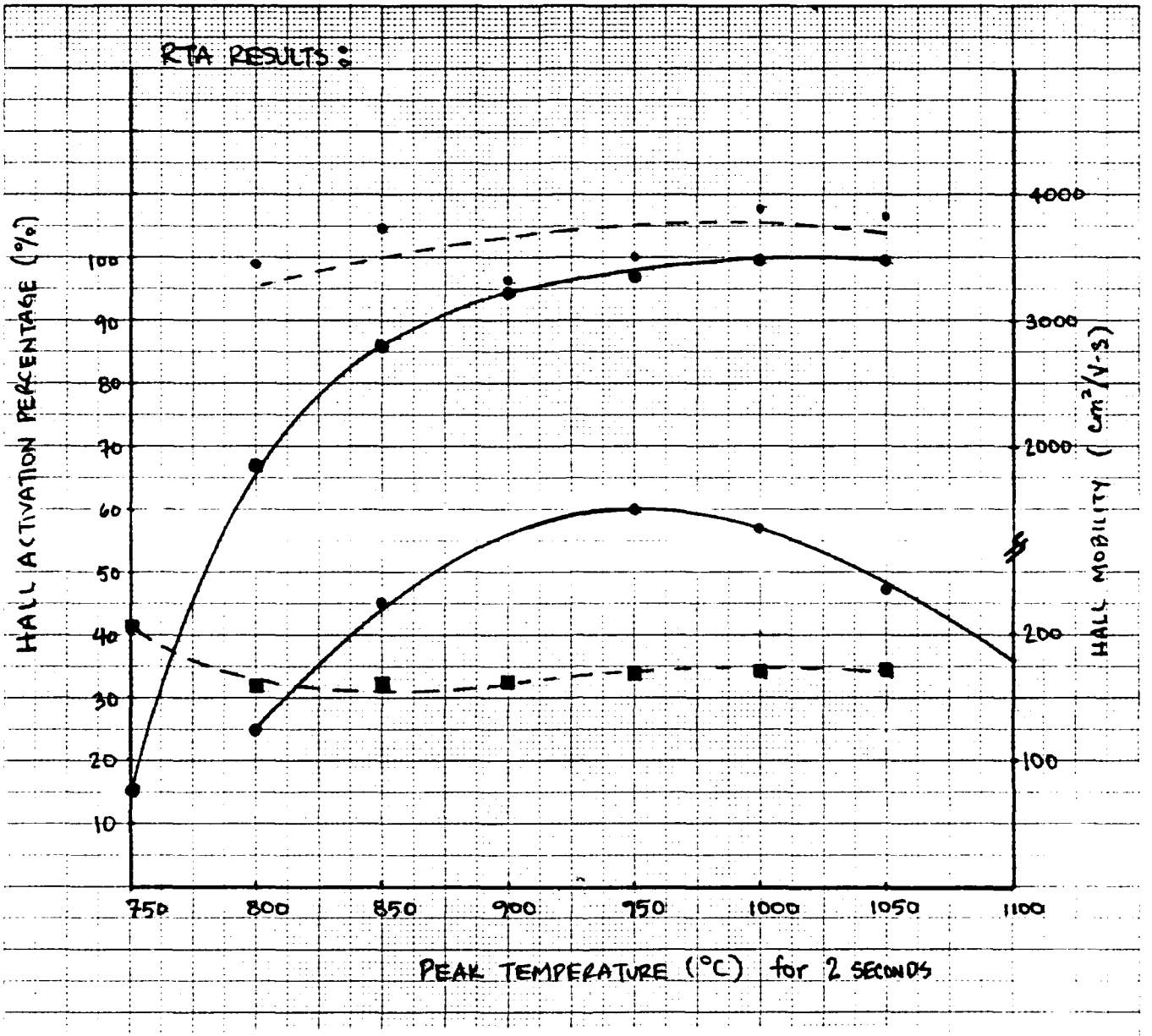


Fig. A.1

amphoteric dopant during RTA without an arsenic (As) overpressure. Some of the Si is then incorporated onto As sites and acts as acceptors which reduces the net donor density. This correlates with the above observation that the Hall mobility is the same even though the measured doping level is not. For p-type (Be) the RTA samples had nearly full activation (100%) while FA samples were closer to 80% activation. Again the Hall mobility was independent of the annealing method. A summary of Hall results has been provided in Fig. A.2. Also included is a I-V characteristic for a MESFET fabricated on FA material. Initial devices fabricated on RTA and FA material have shown good device characteristics.

(Si) ACTIVATION % HALL MOBILITY (Be) ACTIVATION % HALL MOBILITY

RTA RESULTS:



FA MESFET

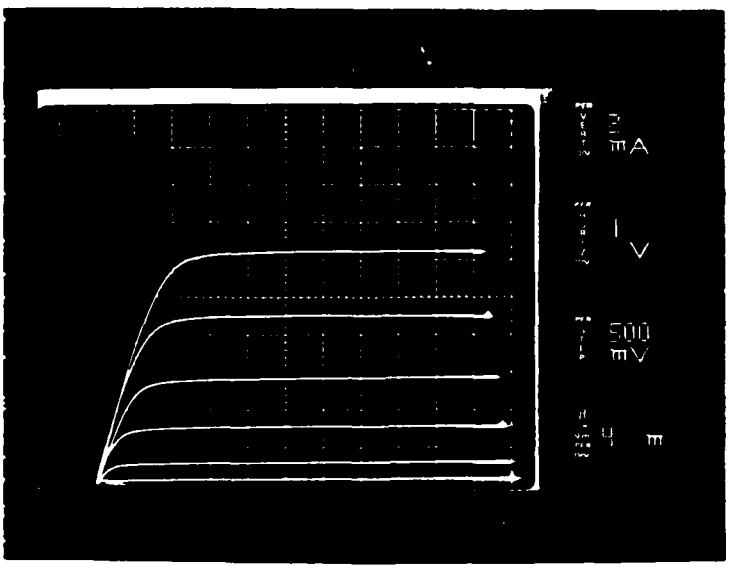


Fig. A.2

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Appendix B

(In,Ga)P/GaAs HBT Fabrication

Preliminary studies on MBE growth of (In,Ga)P on GaAs began at UCSB in 1983 with funding from a UC MICRO Project.* During the past year, HBTs were fabricated from this material and operation of an (In,Ga)P/GaAs HBT was observed for the first time. This MICRO project has goals which are complementary and supportive of the AFOSR project, so the present status of this preliminary work will be included in this report in the form of a preprint of a paper submitted for publication. During the third year of the AFOSR project, (In,Ga)P/GaAs HBT growth and fabrication will be supported by AFOSR with reduced emphasis on (Aℓ,Ga)As/GaAs HBT work.

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* Jointly funded by a "MICRO" grant from Univ. of California, Hewlett-Packard Corp., Rockwell International and Xerox Corp. Prof. H. Kroemer is the principal investigator.

Heterojunction Bipolar Transistor Using a (Ga,In)P Emitter on a GaAs Base, Grown by Molecular Beam Epitaxy

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Abstract

We report the first Npn heterojunction bipolar transistor (HBT) using a (Ga,In)P/GaAs heterojunction emitter. The structure was grown by molecular beam epitaxy, with the base doping exceeding the n-type Si doping of the (Ga,In)P wide gap emitter (E_g= 1.88 eV). Common-emitter gains of 30 were attained at a current density of 3000 A/cm^2. The theoretical energy band lineup of the (Ga,In)P/GaAs heterojunction (valence band offset of 0.29 eV and conduction band offset of 0.16 eV, by the Harrison theory) makes it a potential emitter for high-performance GaAs-based HBTs.

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Introduction

Heterojunction bipolar transistors (HBTs) have stimulated much interest due to their predicted potential for high current gain and high frequency performance [1]. By utilizing an emitter with a wider energy gap than that of the base, the majority carriers of the base can be strongly confined to this region. This confinement leads to a high emitter injection efficiency, relatively independent of the doping levels. Hence, the base can be doped heavily, while the emitter doping may be dropped below the doping levels encountered in the base of a homojunction transistor, and still retain a high injection efficiency. This inversion of doping levels yields reductions in the base resistance and emitter-base capacitance, both essential for high frequency operation. As the technology has been developed, HBTs displaying outstanding characteristics have been realized: molecular beam epitaxy (MBE) grown (Al,Ga)As/GaAs HBTs with unity gain cut-off frequencies of 40 GHz have been reported [2], as well as liquid-phase-epitaxy (LPE) grown (Al,Ga)As/GaAs HBT exhibiting common emitter gains greater than 2000 [3].

The GaAs-based HBT work up to now has concentrated solely on GaAs paired with (Al,Ga)As. This dominance is due to that material system's convenient automatic lattice matching feature, which yields interfaces of low defect densities. With regard to the energy band line-up in the (Al,Ga)As/GaAs system, however, the pair is less than ideal because of the unfavorable band line-up: about 62% of the energy gap difference occurs in

the conduction band [4], causing an undesirable potential barrier to electron injection from the emitter [1]. Although compositional grading of the emitter has been demonstrated to alleviate this drawback [5], a heterojunction with a majority of its energy gap discontinuity in the valence band would be much more desirable.

The (Ga,In)P/GaAs system has been proposed as such an alternate for GaAs-based HBTs [6]. Using the predictions of the Harrison theory [7], a linear interpolation between the band offsets of the GaP/GaAs and InP/GaAs heterojunctions yields a valence band offset of 0.29 eV and a conduction band offset of 0.16 eV for the lattice-matched $Ga_{0.51}In_{0.49}P$/GaAs heterojunction. In this letter, we present what we believe to be the first report on the fabrication of a (Ga,In)P/GaAs HBT, and the demonstration of the wide-gap emitter effect in this device.

MBE Growth and Device Fabrication

The epitaxial layers of the HBT reported here were grown by MBE in a Varian 360 system. A (100)-oriented GaAs substrate, Si-doped to 10^{18} cm^{-3}, was used. At a substrate temperature of 560°C, a 0.25 μm thick GaAs collector, non-intentionally doped n-type to 10^{16} cm^{-3}, was grown directly on the substrate, followed by a 0.15 μm thick GaAs base Be-doped p-type to 10^{19} cm^{-3}. The MBE technology of the (Ga,In)P/GaAs system is relatively undeveloped [8,9] with lasers being the only kind of device reported so far [10]. In our procedure, separate Ga and In sources and a novel P_2

source were utilized to grow the (Ga,In)P emitter layer. The P_2 source consisted of a GaP decomposition source [11], modified with a baffle to condense out the undesired Ga flux [12]. Once proper Ga and In fluxes were obtained, as determined by ion gauge measurements at the substrate position, the substrate temperature was set to 510°C. Using a P_2 beam of $3x10^{-6}$ torr, a 0.4 μm thick $Ga_{0.51}In_{0.49}P$ layer, Si-doped n-type to $5x10^{17}$ cm^{-3}, was grown at a rate of 0.5 μm/hr. The Si doping was then increased to 10^{18} cm^{-3} for another 0.1 μm, or ohmic contact to the emitter. Note that the base doping exceeded that of the emitter by over an order of magnitude.

Discrete transistors with relatively large lateral dimensions were fabricated from the grown wafer using the mesa structure in figures 1(a) and (b). The reason for the large dimensions was to keep the processing as simple as possible. The emitter was contacted with evaporated Au-Ge-Ni. The emitter mesa was then defined by selectively etching down to the GaAs base with HCl. Au-Zn base contacts were evaporated to the exposed p-type GaAs, and the base mesa was etched using $H_2SO_4:H_2O_2:H_2O=10:3:87$. The contacts were then alloyed at 450°C for 1 minute in a $H_2:N_2=15:85$ gas mixture. The collector was contacted with In on the backside of the substrate, which thus served as a portion of the device. The emitter-base junction area was $3.2x10^{-5}$ cm^2. The base-collector junction area was $9.6x10^{-5}cm^2$.

Results and Discussion

A typical I-V characteristic of the p-GaAs/N-(Ga,In)P base/emitter heterojunction is shown in figure 2(a). The diodes have 1.0 volt forward turnon voltages, with hard breakdown between 12 and 14 volt reverse bias.

In figure 2(b), the common-emitter characteristics of a typical HBT are shown. It can be seen that the current gain attains a value of 30 at a maximum collector current of 85 mA, the largest current possible before burnout. As plotted in figure 3, the current gain increases with increasing emitter current, which appears common for HBTs [13]. No gain leveling or roll-off was observed. In fact, the positive slope of β versus current density in figure 3 means that larger current gains would have been achieved if emitter current densities greater than $3x10^3$ A/cm^2 had been possible.

The current densities used in testing the HBTs were limited by what appeared to be "forward secondary breakdown" [14], leading to a burning-out of the device. Device failure was characterized by the collector shorting to the emitter. The shorted emitter/collector combination showed degraded but still rectifying I-V characteristics against the base. The formation of the short circuit was often preceded by gain instability, symptomatic of thermal effects. Power calculations assuming uniform dissipation suggest a junction temperature less than 65°C at room temperature ambient. Hence, the heating is attributed to localized thermal runaway, perhaps caused by localized defects at the (Ga,In)P/GaAs interface.

The relatively large geometries of the devices prevented the determination of the high frequency characteristics. The dc performance was also degraded by the large dimensions of the device, which caused emitter current crowding effects.

The current gain of this non-optimized HBT is at present far below the gains achieved with the more highly developed (Al,Ga)As/GaAs material system [3,5,13], but is comparable to the first (Al,Ga)As/GaAs HBT reported [15]. As indicated, the current-gain-versus-emitter-current-density characteristics of figure 3 imply that higher gains than 30 may be achieved, but the failure mechanism indicates that materials problems still exist. Further improvement of the growth parameters, particularly an increase of the substrate temperature, is expected to increase the injection efficiency and current handling capabilities of the (Ga,In)P/GaAs heterojunctions.

Acknowledgments

The authors are grateful to B.R. Hancock for numerous discussions and for supplying the mask set, to S. Subbanna for performing photoluminescence measurements, to W.E. Gardner for providing x-ray analysis, to Dr. E.J. Caine for many useful discussions, and to D. Zak for his technicial assistance. This work was supported by a grant from Hewlett-Packard, Rockwell, and Xerox, under the University of California MICRO program.

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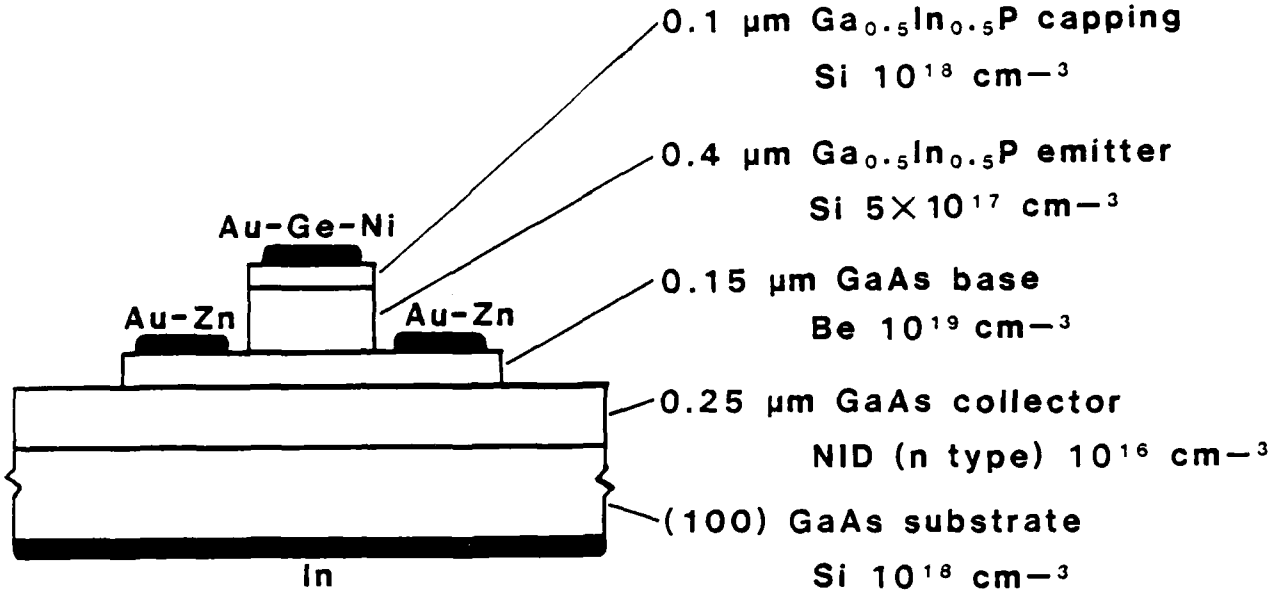
Figure Captions

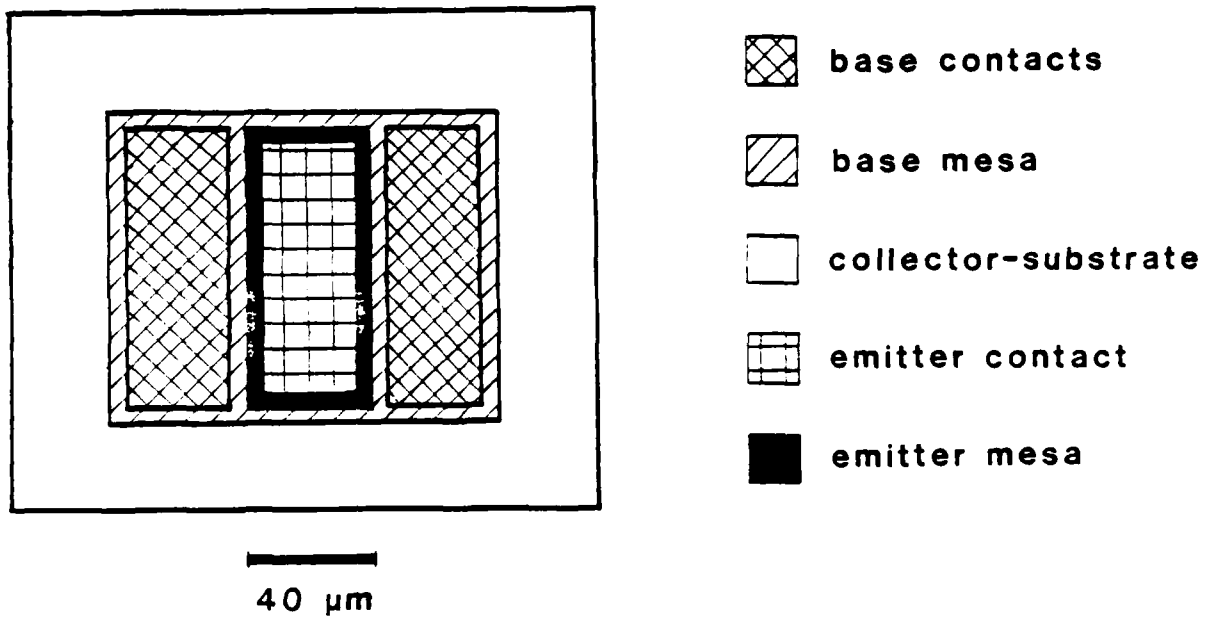
Figure 1- Heterojunction bipolar transistor (a) schematic cross-section (b) scaled top view.

Figure 2- (a) I-V characteristics of GaAs/(Ga,In)P p-N base/emitter heterojunction (b) common emitter characteristics of (Ga,In)P/GaAs heterojunction bipolar transistor.

Figure 3- Common emitter current gain versus emitter current density

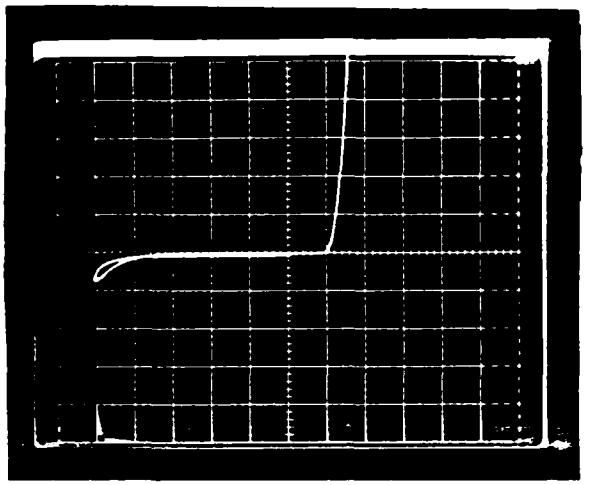

0.1 μm $Ga_{0.5}In_{0.5}P$ capping
Si 10^{18} cm^{-3}
0.4 μm $Ga_{0.5}In_{0.5}P$ emitter
Si 5×10^{17} cm^{-3}
Au-Ge-Ni
Au-Zn
Au-Zn
0.15 μm GaAs base
Be 10^{19} cm^{-3}
0.25 μm GaAs collector
NID (n type) 10^{16} cm^{-3}
(100) GaAs substrate
Si 10^{18} cm^{-3}
In

(a)

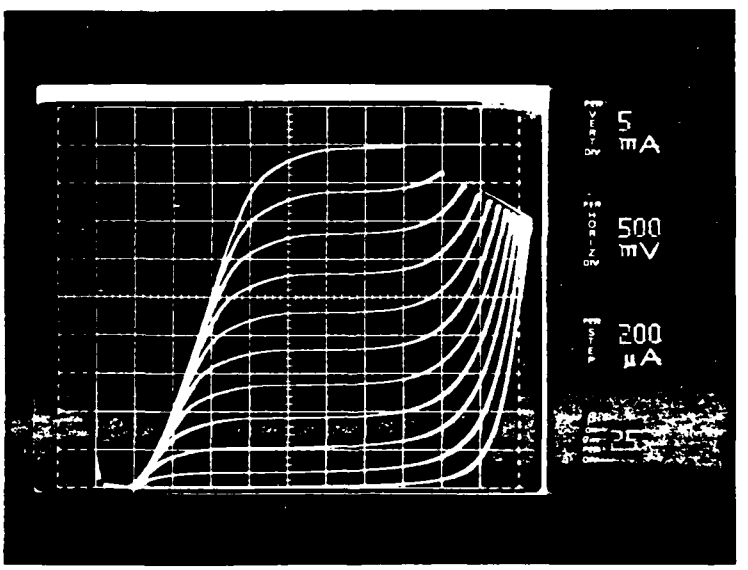

base contacts
base mesa
collector-substrate
emitter contact
emitter mesa
40 μm

(b)

Figure 1



(a)



(b)

Figure 2

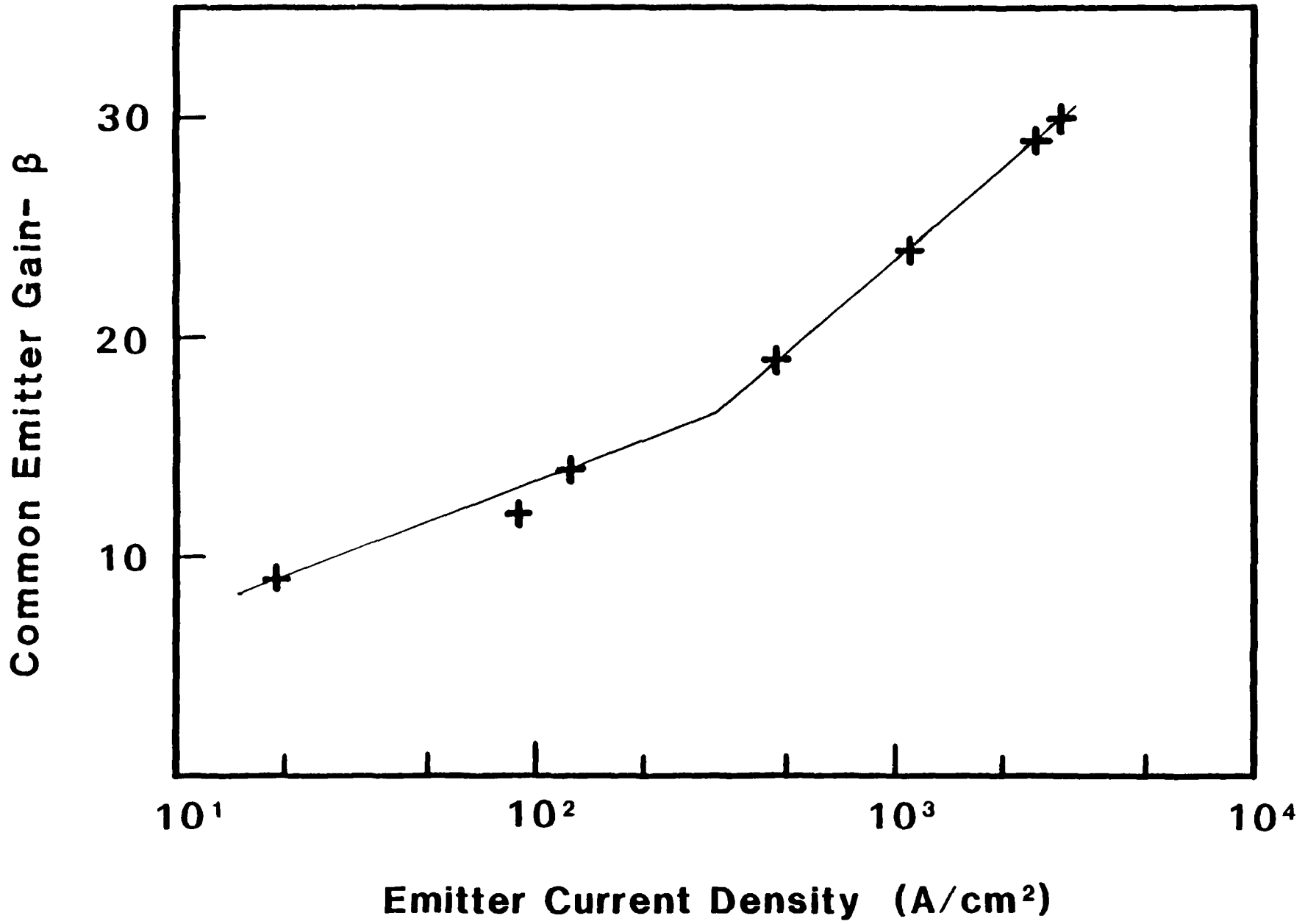

Common Emitter Gain- β
30
20
10
10¹
10²
10³
10⁴
Emitter Current Density (A/cm²)

Figure 3

END

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